

## REMARKS

Claims 1-25 and 42-58 are pending in the application.

Claims 26-41 were previously pending in this application. Claims 26-41 stand withdrawn as non-elected responsive to a restriction requirement and are hereby cancelled without prejudice for presentation in a divisional application.

Claims 20-25, 48 and 49 are allowed.

Claims 1, 2, 4-11, 42-46, 50-58 are rejected.

Claims 3, 12-19 and 42 are objected to.

Claims 1, 2, 4, 6, 7, 9-11, 42, 45, 46, 50, 51 and 54-58 are rejected under 35 U.S.C. 102(a).

Claims 5, 8, 44, 52 and 53 are rejected under 35 U.S.C. 103(a).

Claims 1, 42, 44, and 45 are amended.

Claim 3, which is indicated as allowable, is cancelled in favor of amended claims 1, 42, 44 and 45.

No new matter is added.

Applicant filed the preliminary amendment with claims 50-58 on January 21, 2004 before the issuance of the first action dated March 31, 2004. Please see Exhibit A, which shows a copy of the preliminary amendment and a fax confirmation. Applicant respectfully requests that the Examiner remove the finality of the action issued on June 8, 2004.

Claims 1-2, 4-20, 42-47 and 50-58 remain in the case for reconsideration.

Applicant requests reconsideration and allowance of the claims in light of the above amendment and following remarks.

### ***Allowable Subject Matter***

Applicant thanks the Examiner for indicating that Claims 3, 12-19 and 47 would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. Claims 20-25, 48 and 49 are allowed.

### ***Claim Rejections – 35 USC 102***

Claims 1, 2, 4, 6, 7, 9-11, 42, 45, 46, 50, 51 and 54-58 are rejected under 35 U.S.C. 102(a) as being anticipated by U.S. Pat. No. 6,664,186 to Callegari et al (“Callegari”).

Applicant respectfully traverses the rejections.

Independent claims 1, 42 and 45 are amended to recite, “the high-k dielectric layer has a dielectric constant greater than that of the silicate interface layer,” the limitation drawn

from allowable claim 3. Therefore, amended independent claims 1, 42 and 45 are now patentable. Also, claims 2, 4, 6, 7, 9-11, 46, 50, 51 and 54-55, which respectively depend from amended claims 1, 42 and 45 are also patentable for their dependency and their own merits.

In addition, with respect to claim 56, it recites, "a silicate interface layer having a dielectric constant greater than that of silicon nitride; a high-k dielectric layer overlying the silicate interface layer, wherein the high-k dielectric layer comprises one or more ordered pairs of first and second layers, and wherein the high-k dielectric layer has a dielectric constant greater than that of the silicate interface layer." Thus, claim 56 recites the same limitations as the limitations of allowable claim 1 or allowed claim 20. Thus, claim 56 is patentable and claims 57-58 are allowable for their dependency and their own merits.

### ***Claim Rejections – 35 USC 103***

Claims 5, 8, 44, 52 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Callegari.

Applicant respectfully traverses the rejections.

For the reasons discussed above, claim 44, which now recites, "the high-k dielectric layer has a dielectric constant greater than that of the silicate interface layer," is patentable and claims 5, 8, 52 and 53, which depend from allowable claims 1 and 44, are also allowable.

For the foregoing reasons, reconsideration and allowance of claims 1-2, 4-20, 42-47 and 50-58 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

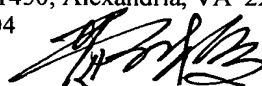
Respectfully submitted,  
MARGER JOHNSON & McCOLLOM, P.C.



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Limited Recognition Under 37 CFR § 10.9(b)

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**Date:** Wednesday, January 21, 2004

Number of pages (including this one): **13**

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**REMARKS:**

Our Docket No. 4591-170; Application No. 09/776,056

Enclosed is a Preliminary Amendment.



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**REMARKS:**

Re: United States Patent Application No. 09/776,059  
DIELECTRIC LAYER FOR SEMICONDUCTOR DEVICE AND METHOD OF  
MANUFACTURING THE SAME  
Our Docket No.: 4591-170

Further to our telephone conversation of April 9, 2004, please review the  
enclosed Preliminary Amendment as filed via fax on January 21, 2004. Please let us  
know if you have any questions.

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PATENT APPLICATION  
Docket No. 4591-170  
Client No. IE10189-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Jong-Ho Lee and Nae-In Lee

Serial No. 09/776,059 Examiner: Douglas Wille

Filed: February 2, 2001 Art Unit: 2814

For: DIELECTRIC LAYER FOR SEMICONDUCTOR DEVICE  
AND METHOD OF MANUFACTURING THE SAME

Confirmation No. 9369

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**PRELIMINARY AMENDMENT**

Prior to Examination, please amend the application as follows.

I hereby certify that this correspondence  
is being transmitted to the U.S. Patent and  
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703-872-9306, on January 21, 2004.

Signature

Adrienne Chochoiak

## IN THE CLAIMS

1. (Original) A multi-layer structure for a semiconductor device, comprising:
  - a silicate interface layer; and
  - a high-k dielectric layer overlying the silicate interface layer.
2. (Original) The multi-layer structure of claim 1, wherein the silicate interface layer has a dielectric constant greater than that of silicon nitride.
3. (Original) The multi-layer structure of claim 1, wherein the high-k dielectric layer has a dielectric constant greater than that of the silicate interface layer.
4. (Original) The multi-layer structure of claim 1, wherein the silicate interface layer is formed of a metal silicate material ( $M_{1-x}Si_xO_2$ ).
5. (Original) The multi-layer structure of claim 4, wherein x is approximately 0.30-0.99.
6. (Original) The multi-layer structure of claim 4, wherein the metal "M" is selected from the group consisting of hafnium (Hf), zirconium (Zr), tantalum (Ta), titanium (Ti) and aluminum (Al).
7. (Original) The multi-layer structure of claim 1, wherein the silicate interface layer is formed by an ALD technique, a MOCVD technique or a reactive sputtering technique.
8. (Original) The multi-layer structure of claim 1, wherein the silicate interface layer is formed to a thickness of approximately 5-10 angstroms.
9. (Original) The multi-layer structure of claim 1, wherein the high-k dielectric layer is a metal oxide layer.

10. (Original) The multi-layer structure of claim 9, wherein the metal oxide layer is an  $\text{HfO}_2$  layer, a  $\text{ZrO}_2$  layer, a  $\text{Ta}_2\text{O}_3$  layer, an  $\text{Al}_2\text{O}_3$  layer, a  $\text{TiO}_2$  layer, an  $\text{Y}_2\text{O}_3$  layer, or a BST layer, a PZT layer, or combinations thereof.

11. (Original) The multi-layer structure of claim 9, wherein the metal oxide layer is formed using an ALD technique, a MOCVD technique or a reactive sputtering technique.

12. (Original) The multi-layer structure of claim 9, wherein the silicate interface layer is formed of a metal silicate material, and wherein the metal of the silicate interface layer is the same as the metal of the metal oxide layer.

13. (Original) The multi-layer structure of claim 1, wherein the high-k dielectric layer comprises one or more ordered pairs of first and second layers.

14. (Original) The multi-layer structure of claim 13, wherein the first layer is formed of  $\text{HfO}_2$ ,  $\text{Ta}_2\text{O}_3$ ,  $\text{Y}_2\text{O}_3$  or  $\text{ZrO}_2$  and the second layer is formed of  $\text{Al}_2\text{O}_3$ .

15. (Original) The multi-layer structure of claim 13, wherein the first layer has a first fixed charge and the second layer has a second fixed charge opposite that of the first fixed charge.

16. (Original) The multi-layer structure of claim 13, wherein the thickness of the second layer is approximately one half the thickness of the first layer.

17. (Original) The multi-layer structure of claim 16, wherein the first layer is formed to a thickness of approximately 10 angstroms and the second layer is formed to a thickness of approximately 5 angstroms.

18. (Original) The multi-layer structure of claim 13, wherein a total thickness of the second layer is not more than approximately one third of the total thickness of the high-k dielectric layer.

19. (Previously presented) The multi-layer structure of claim 13, wherein the upper most layer of the high-k dielectric layer is  $\text{Al}_2\text{O}_3$ .

20. (Original) A multi-layer structure for a semiconductor device, comprising:

a silicate interface layer having a dielectric constant greater than that of silicon nitride; and

a high-k dielectric layer overlying the silicate interface layer,

wherein the high-k dielectric layer comprises one or more ordered pairs of first and second layers, and wherein the high-k dielectric layer has a dielectric constant greater than that of the silicate interface layer.

21. (Original) The multi-layer structure of claim 20, wherein the silicate interface layer is formed of a metal silicate material ( $\text{M}_{1-x}\text{Si}_x\text{O}_2$ ), the metal "M" being selected from the group consisting of hafnium (Hf), zirconium (Zr), tantalum (Ta), titanium (Ti) and aluminum (Al).

22. (Original) The multi-layer structure of claim 20, wherein the first layer is formed of  $\text{HfO}_2$ ,  $\text{Ta}_2\text{O}_3$ ,  $\text{Y}_2\text{O}_3$  or  $\text{ZrO}_2$  and the second layer is formed of  $\text{Al}_2\text{O}_3$ .

23. (Original) The multi-layer structure of claim 20, wherein the thickness of the second layer is approximately one half the thickness of the first layer.

24. (Original) The multi-layer structure of claim 20, wherein a total thickness of the second layer is not more than approximately one third of the total thickness of the high-k dielectric layer.

25. (Previously presented) The multi-layer structure of claim 20, wherein the upper most layer of the high-k dielectric layer is  $\text{Al}_2\text{O}_3$ .

26. (Withdrawn) A method of forming a multi-layer structure for a semiconductor device, comprising:

forming a silicate interface layer; and

forming a high-k dielectric layer overlying the silicate interface layer.

27. (Withdrawn) The method of claim 26, wherein said forming the high-k dielectric layer comprises:

forming a first layer having a first predefined charge;

forming a second layer overlying the first layer, the second layer having a second predefined charge that is opposite that of the first layer.

28. (Withdrawn) The method of claim 27, wherein the first predefined charge is a negative fixed charge and the second predefined charge is a positive fixed charge.

29. (Withdrawn) The method of claim 27, which further comprises forming one or more first and second layers.

30. (Withdrawn) The method of claim 29, wherein the upper most layer of the high-k dielectric layer is  $\text{Al}_2\text{O}_3$ .

31. (Withdrawn) The method of claim 26, wherein said forming the high-k dielectric layer comprises:

forming a first layer having a first controlled thickness; and

forming a second layer overlying the first layer, the second layer having a second controlled thickness, wherein the first and second controlled thicknesses are in the range of approximately 2-60 angstroms.

32. (Withdrawn) The method of claim 31, wherein a total thickness of the second layer is not more than approximately one third of the total thickness of the high-k dielectric layer.

33. (Withdrawn) The method of claim 31, wherein the second layer is approximately one half the thickness of the first layer.

34. (Withdrawn) The method of claim 31, wherein the first layer is formed of  $\text{HfO}_2$ ,  $\text{Ta}_2\text{O}_3$ ,  $\text{Y}_2\text{O}_3$  or  $\text{ZrO}_2$  and the second layer is formed of  $\text{Al}_2\text{O}_3$ .

35. (Withdrawn) The method of claim 26, wherein the silicate interface layer is formed of a metal silicate material ( $M_{1-x}Si_xO_2$ ).

36. (Withdrawn) The method of claim 35, wherein x is approximately 0.30-0.99, and wherein the metal "M" is selected from the group consisting of hafnium (Hf), zirconium (Zr), tantalum (Ta), titanium (Ti) and aluminum (Al).

37. (Withdrawn) The method of claim 26, wherein said forming the silicate interface layer is performed by an ALD technique, a MOCVD technique or a reactive sputtering technique.

38. (Withdrawn) The method of claim 26, wherein the silicate interface layer is formed to a thickness of approximately 5-10 angstroms.

39. (Withdrawn) The method of claim 26, wherein the high-k dielectric layer is a metal oxide layer selected from the group consisting of an  $HfO_2$  layer, a  $ZrO_2$  layer, a  $Ta_2O_3$  layer, an  $Al_2O_3$  layer, a  $TiO_2$  layer, an  $Y_2O_3$  layer, a BST layer, a PZT layer, and combinations thereof.

40. (Withdrawn) The method of claim 39, wherein the metal oxide layer is formed using an ALD technique, a MOCVD technique or a reactive sputtering technique.

41. (Withdrawn) The method of claim 39, wherein the silicate interface layer is formed of a metal silicate material, and wherein the metal of the silicate interface layer is the same as the metal of the metal oxide layer.

42. (Previously presented) A transistor comprising:  
a substrate;  
a silicate interface layer formed over the substrate; and  
a high-k dielectric layer formed over the silicate interface layer;  
a gate formed over the high-k dielectric layer; and  
a source/drain region formed adjacent the gate.

43. (Original) The transistor of claim 42, wherein an upper most portion of the high-k dielectric layer is  $\text{Al}_2\text{O}_3$ , and wherein said gate comprises poly-silicon.

44. (Original) A non-volatile memory, comprising:  
a substrate;  
a floating gate overlying the substrate;  
a silicate interface layer formed over the floating gate;  
a high-k dielectric layer formed over the silicate interface layer; and  
a control gate overlying the high-k dielectric layer.

45. (Previously presented) A capacitor for a semiconductor device, comprising;  
a lower electrode;  
a silicate interface layer formed over the lower electrode;  
a high-k dielectric layer formed over the silicate interface layer; and  
an upper electrode formed over the high-k dielectric layer.

46. (Previously presented) The multi-layer structure of claim 1, wherein the multi-layer is used for a capacitor between a lower electrode and an upper electrode.

47. (Previously presented) The multi-layer structure of claim 14, wherein the multi-layer is used for a capacitor between a lower electrode and an upper electrode.

48. (Previously presented) The multi-layer structure of claim 20, wherein the multi-layer is used for a capacitor between a lower electrode and an upper electrode.

49. (Previously presented) The multi-layer structure of claim 22, wherein the multi-layer is used for a capacitor between a lower electrode and an upper electrode.

50. (New) The transistor of claim 42, wherein the silicate interface layer is formed of a metal silicate material ( $M_{1-x}Si_xO_2$ ), the metal "M" being selected from the group consisting of hafnium (Hf), zirconium (Zr), tantalum (Ta), titanium (Ti) and aluminum (Al).

51. (New) The transistor of claim 42, wherein the high-k dielectric layer comprises one or more ordered pairs of first and second layers, and wherein the first layer is formed of  $HfO_2$ ,  $Ta_2O_3$ ,  $Y_2O_3$  or  $ZrO_2$  and the second layer is formed of  $Al_2O_3$ .

52. (New) The non-volatile memory of claim 44, wherein the silicate interface layer is formed of a metal silicate material ( $M_{1-x}Si_xO_2$ ), the metal "M" being selected from the group consisting of hafnium (Hf), zirconium (Zr), tantalum (Ta), titanium (Ti) and aluminum (Al).

53. (New) The non-volatile memory of claim 44, wherein the high-k dielectric layer comprises one or more ordered pairs of first and second layers, and wherein the first layer is formed of  $HfO_2$ ,  $Ta_2O_3$ ,  $Y_2O_3$  or  $ZrO_2$  and the second layer is formed of  $Al_2O_3$ .

54. (New) The capacitor of claim 45, wherein the silicate interface layer is formed of a metal silicate material ( $M_{1-x}Si_xO_2$ ), the metal "M" being selected from the group consisting of hafnium (Hf), zirconium (Zr), tantalum (Ta), titanium (Ti) and aluminum (Al).

55. (New) The capacitor of claim 45, wherein the high-k dielectric layer comprises one or more ordered pairs of first and second layers, and, wherein the first layer is formed of  $HfO_2$ ,  $Ta_2O_3$ ,  $Y_2O_3$  or  $ZrO_2$  and the second layer is formed of  $Al_2O_3$ .

56. (New) A capacitor, comprising:  
a lower electrode;

a high-k dielectric layer overlying the silicate interface layer,  
wherein the high-k dielectric layer comprises one or more ordered pairs of first and second layers, and wherein the high-k dielectric layer has a dielectric constant greater than that of the silicate interface layer; and  
an upper electrode.

57. (New) The capacitor of claim 56, wherein the silicate interface layer is formed of a metal silicate material ( $M_{1-x}Si_xO_2$ ), the metal "M" being selected from the group consisting of hafnium (Hf), zirconium (Zr), tantalum (Ta), titanium (Ti) and aluminum (Al).

58. (New) The capacitor of claim 56, wherein the first layer is formed of  $HfO_2$ ,  $Ta_2O_3$ ,  $Y_2O_3$  or  $ZrO_2$  and the second layer is formed of  $Al_2O_3$ .

**REMARKS**

New claims 50-58 are added. No new matter is added.

The Examiner is requested to call the undersigned if any questions arise concerning the above-mentioned application.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

A handwritten signature in dark ink, appearing to read 'A. T. McCollom', is written over a horizontal line.

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